GSM Power-Management System

FEATURES

- Handles all GSM baseband power management
- Input range 2.8V to 5.5V
- Charger input up to 15V
- Seven LDOs optimized for specific GSM subsystems
- High operating efficiency and low stand-by current
- Li-Ion and NiMH battery charge function
- SIM card interface
- Three open-drain output switches to control the LED, alerter and vibrator
- Thermal overload protection
- Under-voltage lock-out protection
- Over-voltage protection
- Power-on reset and start-up timer
- QFN-48 package

APPLICATIONS

- GSM/GPRS Mobile Handsets
- Basic and High-end Phones

DESCRIPTION

The SS8000 is a power-management system chip optimized for GSM handsets. It contains seven LDOs, one to power each of the critical GSM sub-blocks.

Sophisticated controls are available for power-up during battery charging, keypad interface, and RTC alarm. The SS8000 is optimized for maximum battery life featuring a ground current of only 107µA in standby and 187µA when the phone is in operation.

The SS8000 battery charger can be used with lithium ion (Li-Ion) and nickel metal hydride (NiMH) batteries.

The SS8000 contains three open-drain output switches for LED, alerter and vibrator control. The SIM interface provides the level shift between SIM card and microprocessor.

The SS8000 is available in a 48-pin QFN package. The operating temperature range is from -25°C to +85°C.

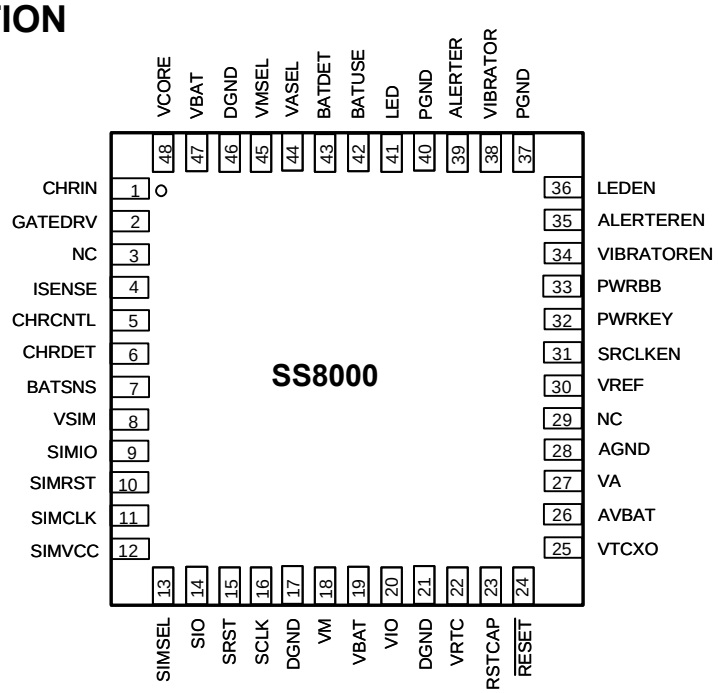
This device is supplied with a Pb-free lead finish (second-level interconnect).

ORDERING INFORMATION

SS8000GQXX

- Packing:
  - TR: Tape and reel
  - TY: Tray
- Package type
  - GQ: QFN-48L, Pb-free lead finish

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

CHRIN and GATEDRV relative to GND……-0.3V to 15V
All other pins relative to GND……-0.3V to 7V
Operating Temperature Ranges……-25°C to +85°C
Maximum Junction Temperature……+165°C
Storage Temperature Range……-65°C to +165°C
Thermal Impedance, θ_{JA} ……23°C/W
Lead Temperature (soldering, 10sec)……+260°C

ELECTRICAL CHARACTERISTICS

(Vbat = 3V-5.5V, CVa=10µF, CVcore =CVm=4.7㎌, CVrtc=0.22µF, CVref=CVtcxo=CVsim=CVio=1µF, minimum loads applied on all outputs, unless otherwise noted. Typical values are at T_A=+25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Main Controller					
Battery Input Voltage Range		3		5.5	V
Charger Input Voltage Range				15	V
Shutdown Supply Current	Vbat<2.5V 2.5V<Vbat<3.2V 3.2V<Vbat		5 30 45	20 55 80	µA
Operation Ground Current	All Output on Vtcxo off, all others on Va, Vtcxo off, all others on		187 148 108	500 200 150	µA
UVLO on Threshold	Vbat	3.15	3.18	3.2	V
UVLO Hysteresis	Vbat		200		mV
Deep Discharging Lockout on Threshold			2.6		V
Deep Discharging Lockout Hysteresis			100		mV
Thermal Shutdown Threshold			165		°C
Thermal Shutdown Hysteresis			25		°C
LDO Enable Response Time			250		µs
Power Key Input High Voltage	PWRKEY	0.7xVbat			V
Power Key Input Low Voltage	PWRKEY			0.3xVbat	V
PWRBB Input High Voltage	PWRBB	1			
PWRBB Input Low Voltage	PWRBB			0.2	
Control Input High Voltage	VMSEL,SIMSEL,SIMVCC,SRCLKEN,VASEL,	2			V
Control Input Low Voltage	BATUSE,LEDEN,VIBRATOREN,ALERTEREN			0.5	V
Digital Core Voltage LDO (Vcore)					
Output Voltage		1.7	1.8	1.9	V
Output Short Current Limit			430		mA
Load Regulation	0.05mA < I_load< 200mA		1.3	10	mV
Line Regulation	3.2V < Vbat < 5.5V		3.3	5	mV
Digital IO Voltage LDO (Vio)					
Output Voltage		2.7	2.8	2.9	V
Output Short Current Limit			275		mA
Load Regulation	0.05mA<I_load<100mA at Vbat=3.6V		3	10	mV
Line Regulation	3.2V<Vbat<5.5V		4.6	5	mV
Analog Voltage LDO (Va)					
Output Voltage		2.7	2.8	2.9	V
Output Short Current Limit			400		mA
Load Regulation	0.05mA<I_load<150mA at Vbat=3.6V		3.3	10	mV
Line Regulation	3.2V<Vbat<5.5V		0.4	5	mV
Output Noise Voltage	Frequency from 10Hz to 100kHz		50		µVrms
Ripple Rejection	Frequency from 10Hz to 3kHz Frequency from 3kHz to 1MHz		65 40		dB
VTCXO Voltage LDO (Vtcxo)					
Output Voltage		2.7	2.8	2.9	V
Output Short Current Limit			45		mA
Load Regulation	0.05mA<I_load<20mA at Vbat=3.6V		0.1	2	mV
Line Regulation	3.2V<Vbat<5.5V		0.4	3	mV
Output Noise Voltage	Frequency from 10Hz to 100kHz		50		µVrms
Ripple Rejection	Frequency from 10Hz to 3kHz Frequency from 3kHz to 1MHz		65 40		dB

ELECTRICAL CHARACTERISTICS (cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RTC Voltage LDO (Vrtc)					
Output Voltage		1.3	1.5	1.65	V
Output Short Current Limit			1.35		mA
Off Reverse Input Current			0.02	1	µA
Memory Voltage LDO (Vm)					
1.8V Output Voltage		1.7	1.8	1.9	V
2.8V Output Voltage		2.7	2.8	2.9	V
Output Short Current Limit			315		mA
Load Regulation(1.8V) Load Regulation(2.8V)	0.05mA<I_load<150mA at Vbat=3.6V		2.7 4.4	10 10	mV
Line Regulation(1.8V) Line Regulation(2.8V)	3.2V<Vbat<5.5V		2.6 2.8	5 5	mV
SIM Voltage LDO (Vsim)					
1.8V Output Voltage		1.65	1.8	1.95	V
3.0V Output Voltage		2.75	3.0	3.1	V
Output Short Current Limit			38		mA
Load Regulation(1.8V) Load Regulation(3.0V)	0.05mA<I_load<20mA at Vbat=3.6V		1 1.7	2 2	mV
Line Regulation(1.8V) Line Regulation(3.0V)	3.2V<Vbat<5.5V		1.2	3 3	mV
Reference Voltage Output					
Reference Voltage			1.235		V
Line Regulation	2.7V<Vbat<5.5V without load		0.3	2	mV
Output Noise Voltage	Frequency from 10Hz to 100kHz		40		µVrms
Ripple Rejection	Frequency at 217Hz	65	75		dB
Reset Generator					
Reset Output High Voltage		Vio-0.5			V
Reset Output Low Voltage				0.2	V
Reset Output Current			1		mA
Reset on Delay Time per unit Cap.			2		ms/nF
LED/Alerter/Vibrator Driver					
Sink Current of LED Driver	Von<0.3V		150		mA
Sink Current of Alerter Driver	Von<0.3V		300		mA
Sink Current of Vibrator Driver	Von<0.5V		250		mA
Battery Charger					
Charge Output Voltage (Li-ion Battery)	BATUSE=0		4.2		V
Charge Output Voltage (NiMH Battery)	BATUSE=1		5.1		V
Chr_Det On Threshold	(Chrin-Vbat)/Vbat , Chrin>4V		3.75		%
Chr_Det Off Threshold	(Chrin-Vbat)/Vbat , Chrin>4V		2.5		%
Pre-charging Current	I_charge@Vbat=3V(UVLO Active), R1=0.2Ω		50		mV
GSM Interface					
Vih(SIMCLK,SIMRST)		Vio-0.6			V
Vil (SIMCLK,SIMRST)				0.6	V
Vilsimio	Vol? 0.4V, Iol=1mA			0.23	V
	Vol? 0.4V, Iol=0mA			0.335	V
Vihsimio , Vohsimio	Iih,Ioh=± 20µA	Vio-0.6			V
Iilsimio	Vil=0V			-0.9	mA
Volsimio	Vil=0.4V			0.42	V
SIMIO Pull-up Resistance to Vio		16	20	24	KΩ

ELECTRICAL CHARACTERISTICS (cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Interface to 3V SIM card					
Volrst	I=20µA			0.4	V
Vohrst	I=-200µA	0.9Vsim			V
Volclk	I=20µA			0.4	V
Vohclk	I=-200µA	0.9Vsim			V
Vil				0.4	V
Vihsio , Vohsio	I=± 20µA	Vsim-0.4			V
Iil	Vil=0V			-1	mA
Vol	Iol=1mA , SIMIO? 0.23V			0.4	V
Interface to 1.8V SIM card					
Volrst	I=20µA			0.2Vsim	V
Vohrst	I=-200µA	0.9Vsim			V
Volclk	I=20µA			0.2Vsim	V
Vohclk	I=-200µA	0.9Vsim			V
Vil				0.4	V
Vihsio , Vohsio	I=± 20µA	Vsim-0.4			V
Iil	Vil=0V			-1	mA
Vol	Iol=1mA , SIMIO? 0.23V			0.4	V
SIM Card Interface Timing					
SIO Pull-up Resistance to Vsim		8	10	12	KΩ
SRST , SIO rise/fall time	Vsim=3/1.8V, load with 30pF			1	µS
SCLK rise/fall time	Vsim=3V, CLK load with 30pF			18	nS
	Vsim=1.8V, CLK load with 30pF			50	nS
SCLK frequency	CLK load with 30pF	5			Mhz
SCLK duty cycle	SIMCLK Duty=50%, fsimclk=5Mhz	47		53	%
SCLK Prop. Delay			30	50	nS

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	CHRIN	Charger Input Voltage
2	GATEDRV	Gate Drive Output
3,29	NC	
4	ISENSE	Charger Current Sense Input
5	CHRCNTL	Microprocessor Control Input Signal for Gate Drive
6	CHRDET	Charger Detect Output
7	BATSNS	Battery Input Voltage Sense
8	VSIM	SIM Supply
9	SIMIO	Non-Level-Shifted Bidirectional Data I/O
10	SIMRST	Non-Level-Shifted SIM Reset Input
11	SIMCLK	Non-Level-Shifted SIM Clock Input
12	SIMVCC	SIM Enable
13	SIMSEL	High for Vsim=3.0V, Low for Vsim=1.8V
14	SIO	Level-Shifted SIM Bidirectional Data Input/Output
15	SRST	Level-Shifted SIM Reset Output
16	SCLK	Level-Shifted SIM Clock Output
17,21,46	DGND	Digital Ground
18	VM	Memory Supply
19	VBAT	Battery Input Voltage
20	VIO	Digital IO Supply
22	VRTC	Real Time Clock Supply
23	RSTCAP	Reset Delay Time Capacitance
24	/RESET	System Reset, Low Active
25	VTCXO	TCXO Supply
26	AVBAT	Battery Input Voltage for Analog Block Circuits
27	VA	Analog Supply
28	AGND	Analog Ground
30	VREF	Reference Voltage Output
31	SRCLKEN	VTCXO and VA Enable
32	PWRKEY	Power on/off Key
33	PWRBB	Power on/off Signal from Microprocessor
34	VIBRATOREN	Vibrator Driver Enable
35	ALERTEREN	Alerter Driver Enable
36	LEDEN	LED Driver Enable
37,40	PGND	Power Ground
38	VIBRATOR	Vibrator Driver Input
39	ALERTER	Alerter Driver Input
41	LED	LED Driver Input
42	BATUSE	Battery Type Selection, High for NiMH, Low for Li-ion
43	BATDET	Battery Detect Output
44	VASEL	High for VA enabled with VTCXO, Low for VA enabled with VD
45	VMSEL	High for Vm=2.8 V, Low for Vm=1.8V
47	VBAT	Battery Input Voltage
48	VCORE	Digital Core Supply

APPLICATION INFORMATION

The SS8000 is a power management chip optimized for use with GSM baseband chipsets in handset applications. Figure 1 shows the block diagram of the SS8000.

Seven low-dropout regulators (core, digital I/O, analog, crystal oscillator, real-time clock, memory, SIM)
SIM card interface
Vibrator, alerter, and LED drivers
Power sequence and protection logic
Reset generator
Under-voltage lockout
Deep discharge lockout
Battery charger

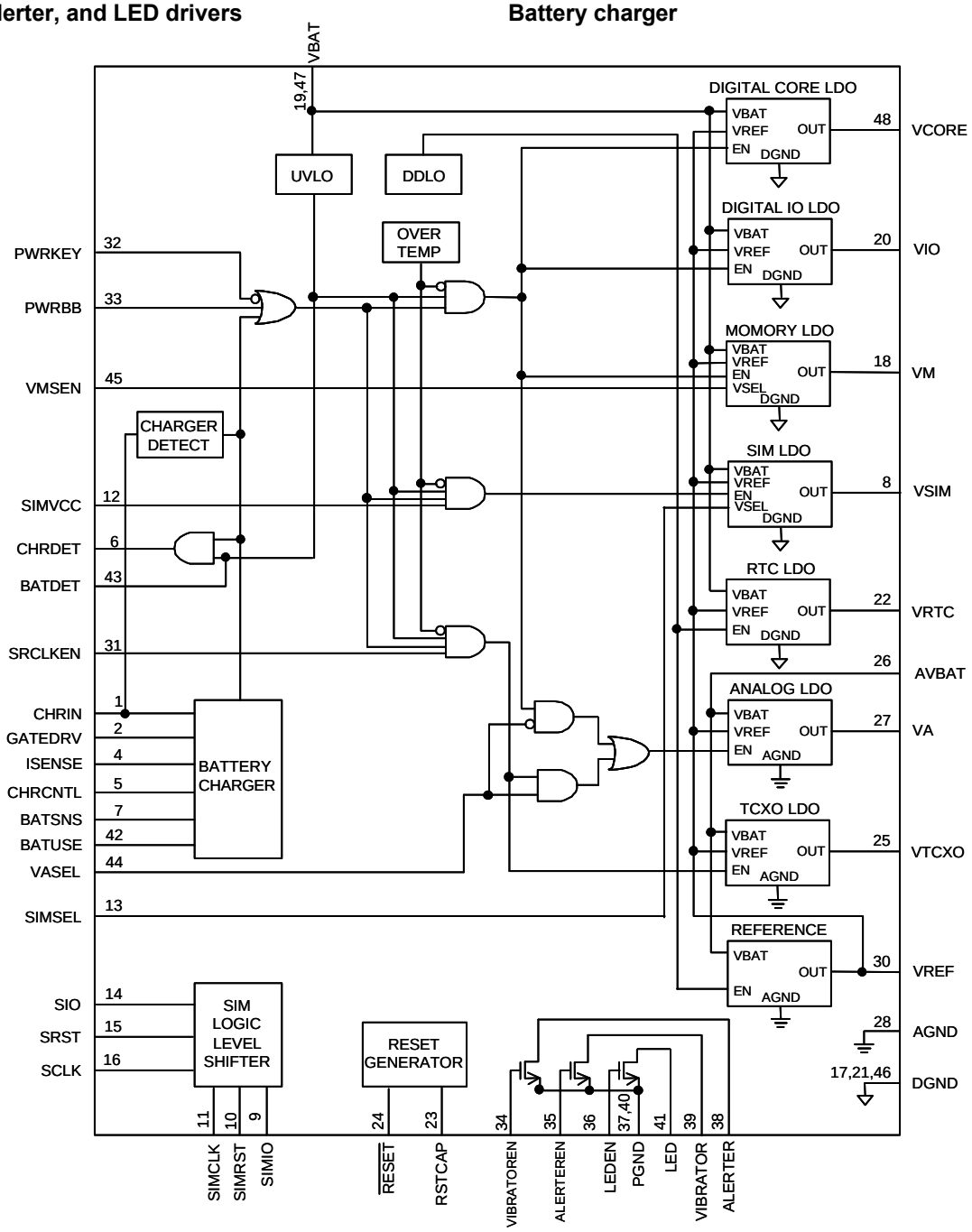


Figure 1. Functional Block Diagram

APPLICATION INFORMATION (cont.)

Low Dropout Regulator (LDOs) and Reference
The SS8000 integrates seven LDOs that are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection, and output noise.

Digital Core LDO (Vcore)
The digital core LDO is a regulator that can source 200mA (max) with 1.8V output voltage. It supplies the baseband circuitry in the handset. The LDO is optimized for very low quiescent current.

Digital IO LDO (Vio)
The digital I/O LDO is a regulator that can source 100mA (max) with 2.8V output voltage. It supplies the baseband circuitry in the handset. The LDO is optimized for very low quiescent current and will power up at the same time as the digital core LDO.

Analog LDO (Va)
The analog LDO is a regulator that can source 150mA (max) with 2.8V output voltage. It supplies the analog sections of the baseband chipsets. The LDO is optimized for low frequency ripple rejection in order to reject the ripple coming from the RF power amplifier burst frequency at 217kHz.

TCXO LDO (Vtcxo)
The TCXO LDO is a regulator that can source 20mA (max) with 2.8V output voltage. It supplies the temperature compensated crystal oscillator, which needs its own ultra low noise supply and very good ripple rejection ratio.

RTC LDO (Vrtc)
The RTC LDO is a regulator that can source 200µA (max) with 1.5V output voltage. It charges up a capacitor-type backup coin cell to run the real-time clock module. The LDO features the reverse current protection and is optimized for ultra low quiescent current since it is always on except when the battery voltage is below 2.5V.

Memory LDO (Vm)
The memory LDO is a regulator that can source 150mA (max) with 1.8V or 2.8V output voltage, selected according to the supply specs of the memory chips. It supplies the memory circuitry in the handset. The LDO is optimized for very low quiescent current and will power up at the same time as the digital core LDO.

SIM LDO (Vsim)
The SIM LDO is a regulator that can source 20mA (max) with 1.8V or 3.0V output voltage, selected according to the supply specs of the subscriber identity modules (SIM) card. It supplies the SIMs in the handset. The LDO is controlled independently of the others LDO.

Reference Voltage Output (Vref)
The reference voltage output is a low noise, high PSRR and high precision reference with a guaranteed accuracy of 1.5% over temperature. It is used as an internal system reference within the SS8000. However, to maintain accurate specs on every LDO output voltage, it is important to avoid loading the reference voltage and it should be bypassed to GND with 100 nF minimum.

SIM Card Interface
The SIM card interface circuitry of the SS8000 meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for the low-voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of the digital IO (Vio) of the baseband chipset to the SIM supply (Vsim). The bi-directional data bus is internally pulled high with a 20kohm resistor on the controller side and with a 10kohm resistor on the SIM side.

All pins that connect to the SIM card (Vsim, SRST, SCLK, SIO) withstand over 5kV of human-body-mode ESD. In order to ensure proper ESD protection, careful board layout is required.

Vibrator, Alerter, LED Switches
Three built-in open-drain output switches drive the vibrator motor, alerter beeper and LEDs in the handset. Each switch is controlled by the baseband chipset with enable pins. The LED switch can sink 150mA to drive up to 10 LEDs simultaneously for backlight. The vibrator switch can sink 250mA for a vibrator motor. The alerter switch can sink 300mA to drive the beeper. All the open-drain output switches are high impedance when disabled.

APPLICATION INFORMATION (cont.)

Power Sequence and Protection Logic
The SS8000 handles the power-ON and -OFF of the handset. It is possible to start the power-on sequence in three different ways:

- Pulling PWRKEY low
- Pulling PWRBB high
- CHRIN exceeds Chr_Det threshold

Pulling PWRKEY low is the normal way of turning on the handset. This will turn on Vcore, Vio, Vm LDOs as long as the PWRKEY is held low. The Vtcxo and Va LDOs are turned on when SRCLKEN is high. The microprocessor then starts and pulls PWRBB high after which the PWRKEY can be released. Pulling PWRBB high will also turn on the handset. This is the case when the alarm in the RTC expires.

Applying an external supply on CHRIN will also turn the handset on. If the SS8000 is in the UVLO state, applying the adapter will not start up the LDOs.

Table 1 shows states of the handset and the LDOs

Table 1. States of Mobile Handset and LDO

Phone State	Chr_on	-UV	PWRBB (–PWRKEY)	SRCLKEN	Vrtc	Vd,Vio,Vm	Va, Vtcxo
No Battery or Vbat < 2.5V	X	L	X	X	Off	Off	Off
2.5V < Vbat < 3.2V	L	L	X	X	On	Off	Off
Pre-Charging	H	L	X	X	On	Off	Off
Charger-on	H	H	X	X	On	On	On
Switched off	L	H	L	X	On	Off	Off
Stand-by	L	H	H	L	On	Off	On
Active	L	H	H	H	On	On	On

Undervoltage Lockout (UVLO)
The UVLO function in the SS8000 prevents startup when initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is greater than 3.2V, the UVLO comparator trips and the threshold is reduced to 3.0V. This allows the handset to start normally until the battery decays to below 3.0V.

Once the SS8000 enters a UVLO state, it draws very low quiescent current, typically 30µA. The RTC LDO is still running until the DDLO disables it. In this mode the SS8000 draws 5µA of quiescent current.

Deep Discharge Lockout (DDLO)
The DDLO in the SS8000 has two functions:

- To turn off the Vrtc LDO.
- To shut down the handset when the software fails to turn off the phone when the battery drops below 3.0V. The DDLO will shut down the handset when the battery falls below 2.5 V to prevent further discharge and damage to the cells.

Reset
The SS8000 contains a reset circuit that is active at both power-up and power-down. The RESET pin is held low at initial power-up, and the reset delay timer is started. The delay is set by an external capacitor on RSTCAP:

$$t_{RESET} = 2\frac{ms}{nF} \times C_{RSTCAP} \quad (1)$$

At power-off, RESET will be kept low.

Over-temperature Protection
If the die temperature of the SS8000 exceeds 165°C, the SS8000 will disable all the LDOs except the RTC LDO. Once the over-temperature state is resolved, a new power-on sequence is required to enable the LDOs.

Battery Charger
The SS8000 battery charger can be used with Li-ion and NiMH batteries. The BATUSE pin can set SS8000 to fit the battery type. BATUSE is set low when a Li-ion battery is used, and set high when a NiMH battery is used. The SS8000 charges the battery in three phases: pre-charging, constant current mode charging, and constant voltage mode charging. Figure 2 shows the flow chart of charger behavior. The circuitry of the SS8000 combines a PMOS transistor, diode, current-sense resistor externally to form a simple and low cost linear charger shown in Figure 3. The SS8000 provides a pulsed top-off charging algorithm through the CHRCNTL pin from the baseband chipset.

APPLICATION INFORMATION (cont.)

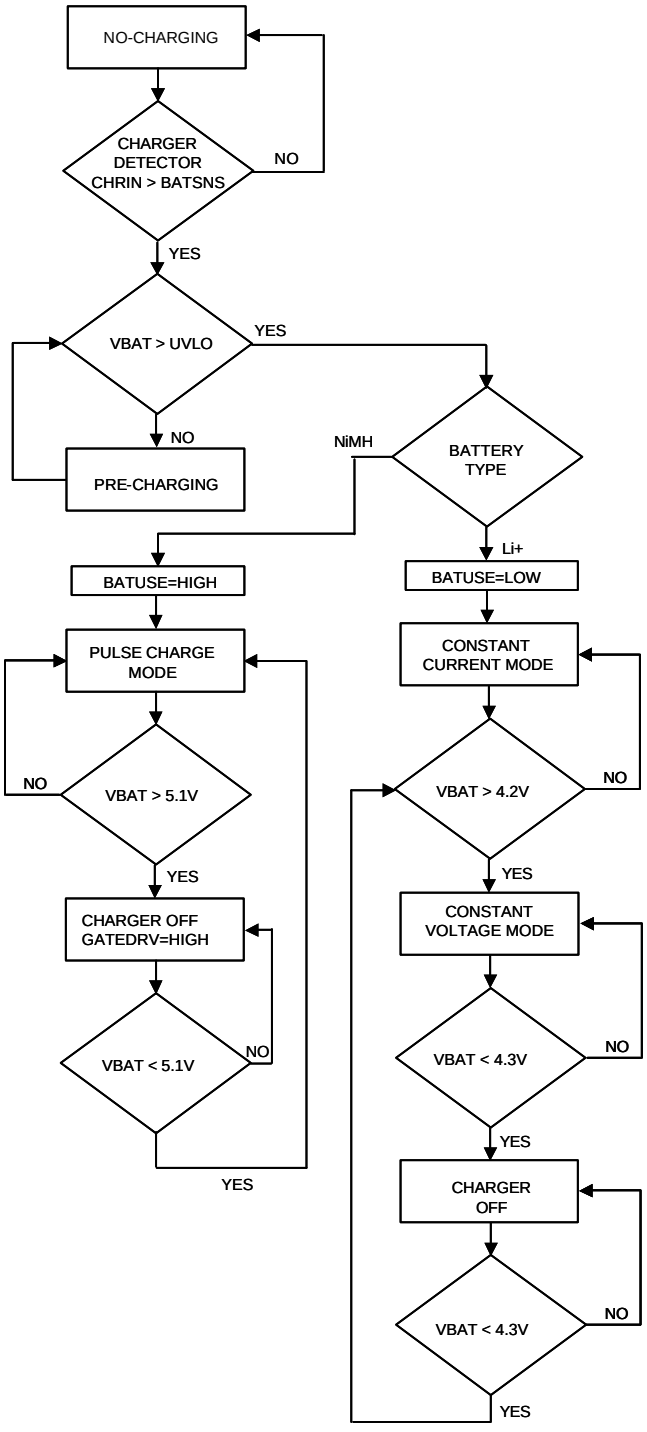


Figure 2. Batter Charger Flow Chart

APPLICATION INFORMATION (cont.)

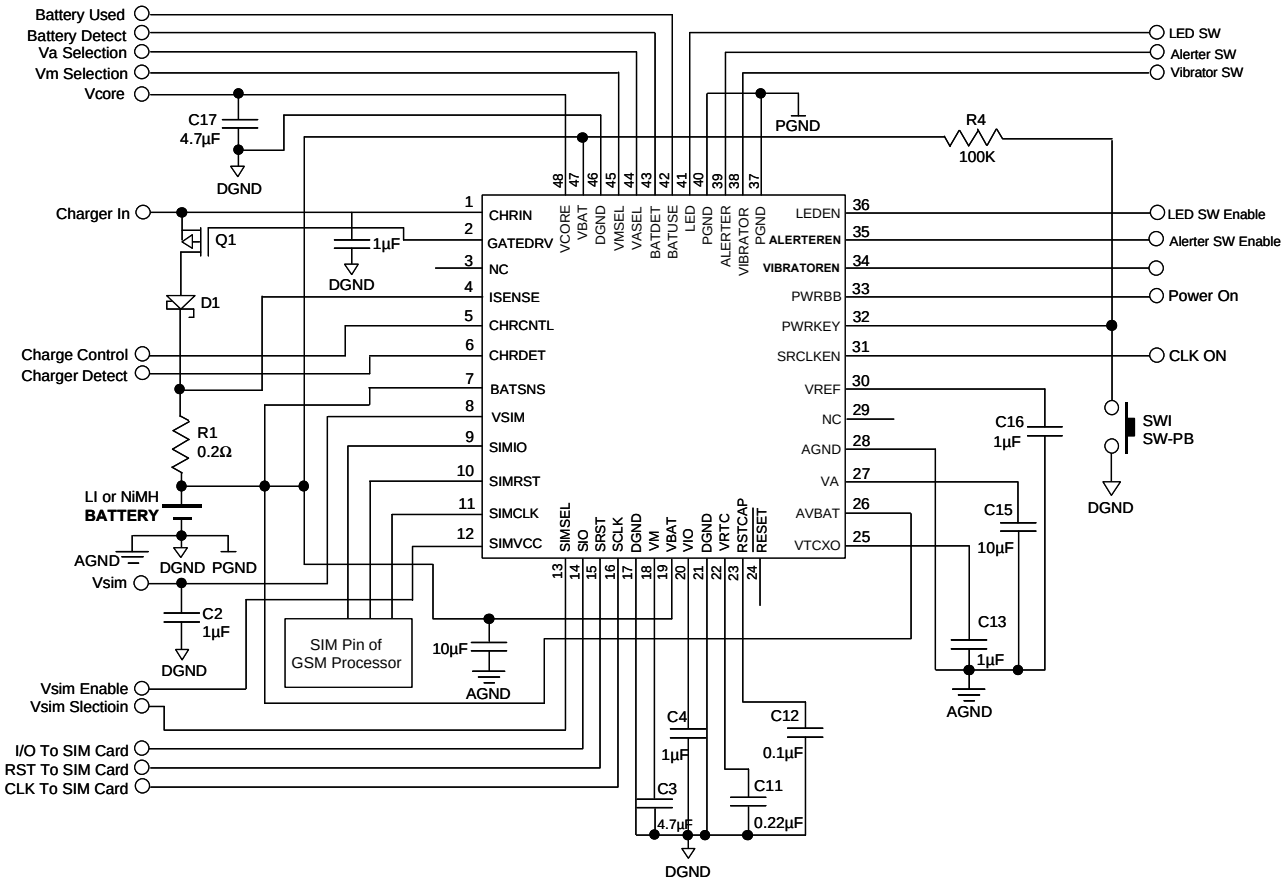


Figure 3. Typical Application Circuit

APPLICATION INFORMATION (cont.)

Charge Detection

The SS8000 charger block has a detection circuit that determines via the CHRIN pin if an adapter has been connected. If the adapter voltage exceeds the battery voltage by 3.75%, the CHRDET output will go high. If the adapter is then removed and the voltage at the CHRIN pin drops to only 2.5% above the VBAT pin, CHRDET goes low.

Pre-Charging mode

When the battery voltage is below the UVLO threshold, the charge current is in the pre-charging mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2V, a 10mA trickle current from the SS8000 charges the battery. When the battery voltage exceeds 2V, the pre-charge current is enabled, which allows 10mV (typically) across the external current sense resistor. This pre-charge current can be calculated:

$$I_{PRE\_CHARGING} = \frac{V_{SENSE}}{R1} = \frac{10mV}{R1} \qquad (2)$$

Constant Current Charging Mode

Once the battery voltage has exceeded the UVLO threshold, the charger will switch to the constant current charging mode. The SS8000 allows 160mV (typically) across the external current sense resistor. This constant current can be calculated.

$$I_{CONSTANT} = \frac{V_{SENSE}}{R1} = \frac{160mV}{R1} \qquad (3)$$

If the battery voltage is below 4.2V when charging a Li-ion battery (5.1V for a NiMH battery), the constant current charging mode is used.

Constant Voltage Charging Mode

This mode only applies to Li-ion battery charging. If the battery has reached the final charge voltage, a constant voltage is applied to the battery and keeps it at 4.2V. This termination of charging is determined by the base-band chip internally, which will pull the CHRCNTL low to stop the charger.

Once the battery voltage exceeds 4.3V for a Li-ion battery (5.1V for a NiMH battery), a hardware over-voltage protection (OV) should be activated to turn off the charger block of the SS8000.

Pulsed Charging Algorithm

The SS8000 provide a pulsed top-off charging algorithm via the CHRCNTL pin. The control signal from the baseband chipset limits the charging duty cycle. This charging algorithm combines the efficiency of switch-mode chargers with the simplicity and low cost of linear chargers.

Battery Voltage Monitor

As Table 2 shows, the relationship between battery voltage and charger control with the corresponding signals is listed. When Vbat <3.2V, an UVB signal is active low. When Vbat >/= 4.3V, an OV signal is active and charging is halted.

Table 2. Charger and Voltage Detection

Vbat	Charger_on	Chr_cntl	Chr_Det Output	-UV	Batuse	Charger Condition
Any Vbat	L	X	L	X	X	No-Charging
Vbat > 3.2V	X	L	X	X	X	No-Charging
Vbat < UV	H	X	H	L	X	Pre-Charging
3.2V<Vbat<4.2V	H	H	H	H	L	CC mode
Vbat = 4.2V	H	H	H	H	L	CV mode
3.2V<Vbat	H	H	H	H	H	CC mode

Notes: OV terminates charging at 4.3V for Li-ion battery or 5.1V for NiMH battery.

APPLICATION INFORMATION (cont.)

External Components Selection

Input Capacitor Selection

For each of the input pins (VBAT) of the SS8000, a 10µF, low ESR capacitor is recommended for local bypass. MLCC capacitors provide the best combination of low ESR and small size. Using a 10µF tantalum capacitor with a small (1µF or 2.2µF) ceramic in parallel is an alternative low cost solution.

For the charger input pin (CHRIN), a 1µF ceramic capacitor is recommended for bypass.

LDO Capacitor Selection

The digital core, analog, and memory LDOs require a 4.7µF capacitor, the digital IO and SIM TCXO LDOs require a 1µF capacitor and the RTC LDO requires a 0.22µF capacitor. Larger value capacitors may be used for improved noise or PSRR performance, but do not forget to consider the settling time that is acceptable for the application. For these, MLCC is recommended.

RESET Capacitor Selection

RESET is held low during power-up for a delay until the LDOs are up. The delay is set by an external capacitor on the RESCAP pin. It can be determined by Eq.(1). A 100nF capacitor will produce a 200ms delay.

Setting the Charge Current

The SS8000 is capable of charging the battery with a charging current programmed by an external sense resistor, Rsen. It is calculated using Eq.(3). If the charge current is defined, Rsen can be found.

Appropriate sense resistors are available from the following vendors: Vishay Dale, IRC, Panasonic.

Charger FET Selection

In selecting the P-channel MOSFET for the charger, consider the minimum drain-source breakdown voltage (BVDS), the minimum turn-on threshold voltage (VGS), and current-handling and power-dissipation capabilities.

Charger Diode Selection

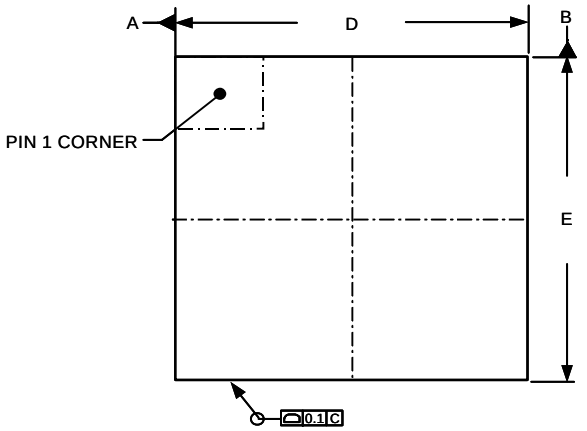
The diode shown in Figure 3 is used to prevent the battery from discharging through the P-channel MOSFETs body-diode into the charger's internal circuits. Choose a diode with a current rating high enough to handle the battery charging current and a voltage rating greater than Vbat.

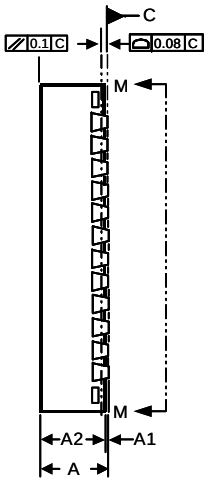
Layout Guidelines

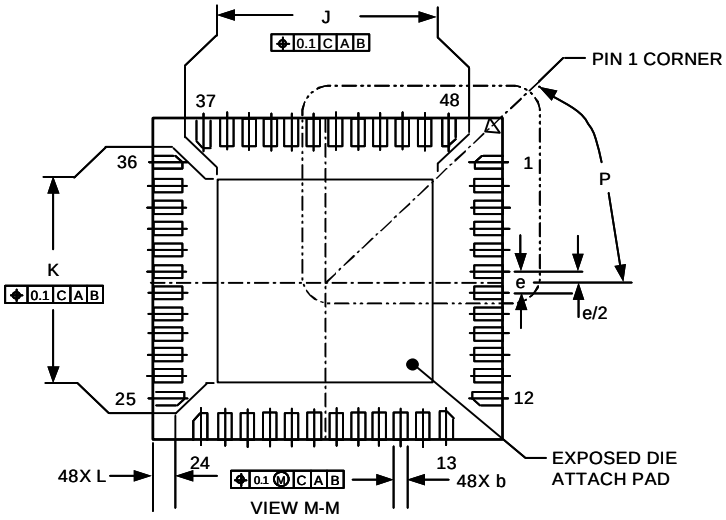
Use the following general guidelines when designing the printed circuit boards:

1. Split the battery connection to the VBAT, AVBAT pins of the SS8000. Locate the input capacitor as close to the pins as possible.
2. Va and Vtcxo capacitors should be returned to AGND.
3. Split the ground connection. Use separate traces or planes for the analog, digital, and power grounds (i.e. AGND, DGND, PGND pins of the SS8000, respectively) and tie them together at a single point, preferably close to the battery return.
4. Run a separate trace from the BATSNS pin to the battery to prevent any voltage drop error in the measurement.
5. Kelvin-connect the charge-current sense-resistor by running separate traces to the BATSNS and ISENSE pins. Make sure that the traces are terminated as close to the resistor's body as possible.
6. Careful use of copper area, weight, and multi-layer construction will help to improve thermal performance.

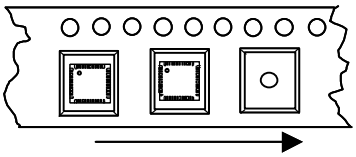
PHYSICAL DIMENSIONS







Taping Specification



Feed Direction
Typical QFN Package Orientation

Note: Coplanarity applies to leads, corner leads and die attach pad.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	-----	1.00	0.031	-----	0.039
A1	0	-----	0.05	0	-----	0.002
A2	0.75	-----	1.00	0.030	-----	0.039
b	0.20	0.25	0.30	0.008	0.010	0.012
D	7 BSC			0.276 BSC		
E	7 BSC			0.276 BSC		
e	0.5 BSC			0.020 BSC		
J	4.50	4.60	4.70	0.177	0.181	0.185
K	4.50	4.60	4.70	0.177	0.181	0.185
L	0.35	0.40	0.45	0.014	0.016	0.018
P	45° REF			45° REF		